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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,989	07/15/2003	Giora Biran	IL920000078US1	8807

54856 7590 05/01/2006

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EXAMINER	
NGUYEN, TANH Q	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 05/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,989	BIRAN ET AL.	
	Examiner	Art Unit	
	Tanh Q. Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Since the petition to have a reference accepted under 37 CFR 1.78(a)(3) is granted, the amendment to the specification filed December 27, 2005 in accordance with 37 CFR 1.78(a)(3) is entered.

Claim Objections

2. Claim 1-10, 17, 18 are objected to because of the following informalities:

"moving the contents of the buffer to the payload portion of the control data block" on line 10 of claim 1 is not underlined, and therefore is not considered proper as added matter. Furthermore, line 8 of claim 1 already recites "moving the contents of the buffer to the payload portion" and claim 1 appears to end at line 9 by the presence of a period.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claims 11-16, 19-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use

the invention. Page 40, lines 3-5 discloses "The payload portion comprises a plurality of fields each containing the identity of the LCP channel that indicated the completion event". It appears that the cited portion only supports a payload portion having a plurality of fields, each corresponding to one of the ports - rather than to a different one of the ports.

In the example of FIG. 18, there are 28 fields in the payload portion. Each field of payload portion contains the identity of the LCP channel (ports) that indicated the completion event (the interrupt) - hence a payload portion having a plurality of fields, each corresponding to one of the ports. The limitation "a plurality of fields each corresponding to a different one of the port" would require 28 different ports, and such limitation appears not to be supported by the specification.

Furthermore, it appears that there is no support for "moving the contents of the buffer to the corresponding fields of the payload portion" - as page 38, lines 25-26 merely discloses "when preset conditions are met, an Interrupt Control Block (ICB) 1680 is generated by the ISOC 120 from the information stored in the interrupt FIFO 1660".

5. Claims 8-10, 17-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites "A peripheral device comprising apparatus claimed in claim 1" in line 1. Since claim 1 also recites "a peripheral device" in line 2, it is not clear whether the peripheral device of claim 8 is the same as the peripheral device of claim 1. Claim 9 recites "A data communication network interface comprising a peripheral device as

claimed in claim 8" in lines 1-2. Since claim 9 depends on claim 8, which depends on claim 1, it is not clear whether the peripheral device recited in claim 9 refers to the peripheral device recited in line 2 of claim 1, or the peripheral device recited in line 1 of claim 8 - if they are not the same. Furthermore, "apparatus" in line 1 of claim 8 should be replaced with "the apparatus", and "a peripheral device" in line 1 of claim 9 should be replaced with "the peripheral device".

Claim 17 recites "A computer program product comprising a computer usable medium having computer readable program code means embodied therein for causing transfer of interrupts, the computer readable program code means...comprising computer readable program code means for causing a computer to effect the functions and all the limitations of claim 1". Since claim 1 is directed to an apparatus, the limitations of claim 1 pertain to the all elements of the apparatus of claim 1. It is not clear how a computer readable program code means can cause a computer to effect all the elements of an apparatus, how a computer program code means can comprise all the elements of an apparatus, or how a computer program product can comprise all the elements of an apparatus.

Claim 18 recites "A computer program product comprising a computer usable medium having computer readable program code means embodied therein for causing data processing, the computer readable program code means...comprising computer readable program code means for causing a computer to effect the functions and all the limitations of claim 10". Since claim 10 is directed to an apparatus, the limitations of claim 10 pertain to the all elements of the apparatus of claim 10. It is not clear how a

computer readable program code means can cause a computer to effect all the elements of an apparatus, how a computer program code means can comprise all the elements of an apparatus, or how a computer program product can comprise all the elements of an apparatus.

Claim 19 recites "An article of manufacture comprising a computer usable medium having computer readable program code means embodied therein for causing transfer of interrupts, the computer readable program code means ...comprising computer readable program code means for causing a computer to effect the steps and all the limitations of claim 11". It is not clear whether the article of manufacture comprises all the limitations of claim 11, or the computer readable program code means comprises all the limitations of claim 11, or a computer readable program code means causes a computer to effect all the limitations of claim 11. Further, it is not clear whether there is any distinction between steps and limitations - in line 4.

Claim 20 recites "A program storage device readable by machine, tangibly embodying a program of instructions...to perform method steps for transferring interrupts, said method steps comprising the steps and all the limitations of claim 11". It is not clear whether there is any distinction between steps and limitations - in line 3. "machine" in line 1 should also be replaced with "a machine".

The rejections that follow are based on the examiner's best interpretation of the claims.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyake et al. (US 5,349,564) in view of Andrews et al. (USP 5,968,158) and further in view of Satran et al. (USP 6,430,183).

9. As per claim 1, Miyake teaches an apparatus [interrupt circuit 4, FIG. 1] for interrupting a host computer system [CPU 2, FIG. 1] by indications of interrupts generated by ports of a peripheral device [RAM 3, FIG. 1; claims 1, 4], the peripheral device having a plurality of ports [ports A, B, C - FIG. 1], the apparatus for transferring interrupts from the peripheral device to the host computer system [col. 1, lines 13-15].

Miyake does not specifically teach a buffer for storing the indications of interrupts.

Andrews teaches a buffer [a distributed buffer 68-0 to 68-7, FIG. 5] for storing indications of interrupts [INT BLOCK 1-INT BLOCK N, FIG. 6; col. 10, lines 60-62] of a peripheral device [10, FIG. 1], and a controller [64-0, FIG. 5; DMA: col. 11, line 51] for, in response to a preset condition being met [col. 11, lines 8-47], generating a control data block [a DMA data block], and sending the contents of the buffer to the host computer system via one of the ports [port connected to PCI BUS 48, FIG. 5] to reduce the overhead for processing the interrupts when compared to processing the interrupts individually [col. 1, lines 39-41].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to store the indications of interrupts in a buffer and to send the indications of interrupts to the host computer system when a preset condition is met, as is taught by Andrews, in order to reduce the overhead for processing the indications of interrupts.

Miyake/Andrews essentially teaches transferring indications of interrupts from the buffer to the host computer system using DMA, instead of using a control data block comprising a payload portion having a plurality of fields each corresponding to one of the ports and a header portion having an identifier for identifying the control data block, moving the contents of the buffer to the fields of the payload portion, and sending the control data block to the host computer system via one of the ports.

Satran teaches a control data block [First Packet Type, FIG. 2] comprising a payload portion [220, 230, FIG. 2] having a plurality of fields [a plurality of block header [220, FIG. 2] and payload data [230, FIG. 2] sections: col. 5, lines 9-15] each

corresponding to a data block to be transmitted, and a header portion [210, FIG. 2] having an identifier [211, FIG. 2] for identifying the control data block [col. 4, lines 17-32], moving the contents of a buffer to the fields of the payload portion [data blocks to be transmitted originating from a single source: col. 4, lines 3-4], and sending the control data block to a receiver [140, FIG. 1] via a port of transmitter [110, FIG. 1].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a control data block, as is taught by Satran, in order to transfer a plurality of indications of interrupts from the peripheral device to a host computer via the port connected to PCI BUS 48 - as an alternative to using DMA to transfer the plurality of indications of interrupts from the peripheral device to a host computer.

10. As per claims 2-4, Andrews teaches the preset condition comprising a determination that the buffer is full [col. 11, lines 22-27: with the predetermined limit being set to the size of the buffer];

the preset condition comprising a determination that at least a predetermined plurality of indications is stored in the buffer and that a predetermined period has elapsed [col. 11, lines 35-40];

the preset condition comprising a determination that at least one indication is stored in the buffer and that a predetermined period has elapsed [col. 11, line 28-35]

11. As per claim 5, Satran does not specifically teach the header portion comprising a count indicative of the number of indications included in the payload portion. Since it was known in the art at the time the invention was made to use a count in a header of a

packet to indicate the number data blocks contained in the packet - for packets with multiple data blocks, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a count in the header portion of the control data block in order to indicate of the number of indications of interrupts included in the payload portion of the control data block.

12. As per claim 6, Satran does not teach the header portion comprising a time of day stamp. Since it was known in the art at the time the invention was made to include a time of day stamp to keep track of the packet processing order to maintain coherency, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a time of day stamp in the header portion of the control data block in order to keep track of the order for processing the control data block.

13. As per claim 7, Andrews teaches the buffer comprising a FIFO memory buffer [col. 10, line 60-col. 11, line 7].

14. As per claim 8, Miyake teaches a peripheral device [RAM 3, FIG. 1] comprising the apparatus [interrupt circuit 4, FIG. 1].

15. As per claim 9, Miyake teaches the peripheral device communicating with processors 8A and 8B. Since it was known in the art at the time the invention was made for processors to communicate with a peripheral device over a network, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the peripheral device to be comprised in a data communication network interface - in order to communicate with the processors over a network.

16. As per claim 10, Miyake teaches an apparatus [1, FIG. 1] comprising a host processing system [2, FIG. 1] having a memory [3, FIG. 1], a data communications interface [ports A, B, C - FIG. 1] for communicating data between the host computer system [through port A] and a data communications network [see rejection of claim 9 above] forming a data processing system [FIG. 1] for controlling flow of interrupts from the data communication interface to the memory of the host computer system.

17. As per claim 11, claim 11 generally corresponds to claim 1, for a specific instance where the buffer contains only one indication of interrupt per port - for a plurality of ports, and the payload portion contains only a number of fields corresponding to the number of ports, each field of the payload portion would correspond to a different one of the ports, and the contents of the buffer are moved to the corresponding fields of the payload portion.

18. As per claims 12-20, claims 12-16 generally correspond to claims 2-5, 7 - and are rejected on the same basis as claims 2-5, 7;

claim 17 generally corresponds to claim 1, and is rejected on the same basis as claim 1;

claim 18 generally corresponds to claim 10, and is rejected on the same basis as claim 10;

claims 19-20 generally correspond to claim 11, and are rejected on the same basis as claim 11.

Response to Arguments

19. Applicant's arguments filed December 27, 2005 have been fully considered but they are not persuasive or moot in view of the new grounds of rejections.

20. With respect to the claim rejections under 35 USC 112, applicant cited "Various communication protocols can be supported simultaneously, with each protocol using a different LCP port", and argued that when there are many protocols, there are many different ports. 28 protocols would have 28 different ports.

The argument is not persuasive because page 40, lines 3-5 discloses "The payload portion comprises a plurality of fields each containing the identity of the LCP channel that indicated the completion event". Such disclosure does not require each of the plurality of fields to correspond to a different one of the ports. It merely requires each of the plurality of fields to correspond to a port. The 28 fields of FIG. 18 do not have to correspond to 28 different ports.

Furthermore, "Various communication protocols can be supported simultaneously, with each protocol using a different LCP port" merely means that several ports can be used simultaneously. Such citation does not require the 28 fields to correspond to 28 different protocols.

21. With respect to the 103 rejections and the teachings of Andrews, applicant's argument is somewhat confusing. It appears that applicant argued that Andrews does not teach a buffer for storing indications of interrupts generated by ports of a peripheral device. The arguments are moot in view of the new grounds of rejections.

22. With respect to the 103 rejections and the teachings of Satran, applicant's

argument is also confusing. It appears that applicant argued that the blocks of Satran are not "control data blocks" in claims 1-20, and that the control data block has "a payload portion".

As Satran teaches a control data block having a payload portion [FIG. 2] and applicant failed to show how the control data block in Satran is different from the control data block in applicant's invention, applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

It also appears that applicant also argued bodily incorporation of the references and/or argued against the references individually. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). Furthermore, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

23. With respect to the 103 rejections and the motivation to combine, applicant argued there is no reason to combine Satran with Andrews, which are apparently unrelated art, except for hindsight. It also appears that applicant argued that the

suggestion to combine must be expressly suggested in any one or all of the references.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In response to applicant's argument that Andrews and Satran are nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, both Andrews and Satran are concerned with how to send data from a source to a destination.

Applicant is also off the mark in arguing that the suggestion to combine must be expressly suggested in any one or all of the references. The measure is what the teachings of the references would suggest to one of ordinary skill in the art, not what the references specifically suggests. See *In re Oetiker*, 24 USPQ2d 1443 (Fed. Cir. 1992)

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Quang Nguyen whose telephone number is (571) 272-4154 and whose e-mail address is tanh.nguyen36@uspto.gov. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh, can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300 for After Final, Official, and Customer Services, or (571) 273-4154 for Draft to the Examiner (please label "PROPOSED" or "DRAFT").

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